WE CLAIM:

1. An interface device for connecting a transmitting device having a first plurality of terminals and deriving a plurality of signals of a predetermined data pattern, the signals being arranged in groups, and a receiving device having a second plurality of terminals for receiving said signals;

the interface device comprising:

input connectors connectable to said transmitter's terminals and output connectors connectable to said receiver's terminals;

a plurality of transmission lines within said interface device, for interconnecting said input and output connectors, the transmission lines being arranged in groups corresponding to said groups of signals; and

a nonvolatile memory for storing data on timing errors in each said group of transmission lines, measured with respect to a reference signal and relating to a specific data pattern;

wherein the transmitting device is capable of compensating for timing errors in said groups of transmission lines using data read from said nonvolatile memory.

2. The interface device of claim 1, wherein said transmission lines in one group are of equal electrical length.

3. The interface device of claim 1, wherein, in case the transmitting device comprises a plurality of registers for driving signals, each register having a respective delay vernier for controlling a separate group of signals, the signals controlled by a separate vernier are fed to a separate group of input connectors.

4. The interface device of claim 1, wherein the data stored in said non-volatile memory comprises data on crosstalk timing errors measured for said groups of signals.

5. The interface device of claim 1, wherein the data stored in said memory comprises data on crosstalk timing errors measured for each signal of the group.

6. The interface device of claim 1, wherein the data stored in said non-volatile memory comprises data on interconnections between said first and second plurality of

terminals and data on crosstalk timing errors in said transmission lines relating to a specific data pattern, for each of said stored interconnection.

7. The interface device of claim 1, wherein the data stored in said non-volatile memory comprises data measured in a series of iterations.

8. The interface device of claim 1, wherein the data are stored in the form of a table containing update values entered during each iteration for centering said groups of signals with respect to the reference signal.

9. A semiconductor device test system having a plurality of terminals and deriving a plurality of signals of a predetermined data pattern, the signals being arranged in groups, to be applied to a semiconductor device under test, the test system comprising an interface device for connecting the test system and the semiconductor device;

the interface device comprising:

input connectors for connecting to said terminals of the test system and output connectors for connecting to said semiconductor device terminals;

a plurality of transmission lines within said interface device, the transmission lines being arranged in groups corresponding to said groups of signals;

and

a nonvolatile memory for storing data on interconnections between said input and output connectors and data on timing errors in each said group of transmission lines measured with respect to a reference signal and relating to a specific data pattern, for each of said stored interconnection;

wherein the test system is capable of compensating for timing errors in said groups of transmission lines using data read from said nonvolatile memory.

10. The system of claim 9, wherein said transmission lines of one group are of equal electrical length.

11. The system of claim 9, wherein said transmission lines of one group are located within one layer of the interface device.

12. The system of claim 9, wherein the transmitting device comprises a plurality of registers for driving signals, each register having a respective delay vernier for controlling a separate group of signals, and the signals controlled by separate verniers are fed to a separate group of transmission lines.

13. The system of claim 9, wherein the transmitting device comprises a plurality of pin cards comprising registers for driving signals, each register having a respective delay vernier, and the signals derived from the separate pin card are fed to a separate group of transmission lines.

14. The system of claim 9, wherein data from crosstalk timing errors are stored with circuit connectivity data in the said nonvolatile memory in the form of a table containing update values entered during current iteration.

15. The system of claim 13, wherein each pin card further comprises a non-volatile memory for storing data on crosstalk timing errors in the said pin card, the test system being capable of compensating for timing errors caused by crosstalk using data read from said nonvolatile memory.

16. The system of claim 9, wherein the transmitter further comprises a non-volatile memory for storing data on crosstalk timing errors in a tester's header, the test system being capable of compensating for timing errors caused by crosstalk using data read from said nonvolatile memory.

17. A method of compensating timing errors in transmission lines comprising the steps of:

- transmitting via transmission lines a plurality of signals of a predetermined data pattern to be applied to a semiconductor device, the signals being driven in groups;

- comparing the output response of a group of signals with a reference signal level;

- storing in a non-volatile memory data on timing errors in said transmission lines relating to specific data patterns, for each separate group of signals; and

- compensating for timing errors in said transmission lines for each said group of signals using said data read from nonvolatile memory.

18. A method of claim 17, wherein the procedure of compensation timing errors is iterative.

19. The method of claim 18, wherein, during the first iteration, the timing errors are measured for groups of signals, each group of signals being controlled by a separate delay vernier of a transmitter's register.

20. The method of claim 18, wherein, during the first iteration, the timing errors are measured for groups of signals, each group of signals relating to a separate pin card.

21. A method of claim 17, wherein, for each group of signals, the leftmost and the rightmost skew value with respect to a reference signal are measured and the whole group of signals is shifted for the average of these two values to adjust its position with respect to the reference signal.

22. The method of claim 17, wherein the timing errors are measured for each bit of a signal.

23. The method of claim 17, wherein, before skew measurements, a clock signal delay is measured to provide high accuracy in subsequent measurements.

24. A method of testing a semiconductor device comprising

- transmitting via transmission lines a plurality of signals of a predetermined data pattern to be applied to said semiconductor device, the signals being arranged in groups;

- comparing the output response of a group of signals with a reference voltage;

- storing in a non-volatile memory data from crosstalk artifacts in said transmission lines relating to specific data patterns, for each separate group of signals; and

- compensating for artifacts caused by crosstalk in said transmission lines for each said group of signals using said data read from said nonvolatile memory.